REMARKS

In response to the Office Action dated June 3, 2009 Applicant respectfully requests reconsideration based on the above claim amendments and the following remarks. Applicant respectfully submits that the claims as presented are in condition for allowance.

Claims 1-11 and 14-17 are pending in the present Application. Claims 1 and 7 are amended, leaving Claims 1-11 and 14-17 for consideration upon entry of the present amendments and the following remarks.

Support for the claim amendments is at least found in the specification, the figures, and the claims as originally filed. Particularly, support for amended Claims 1 and 7 is at least found in originally filed Figures 4 and 6, and in the specification at page 11, lines 9 and 10, page 13, lines 4-23

No new matter has been introduced by these amendments. Reconsideration and allowance of the claims are respectfully requested in view of the above amendments and the following remarks.

Claim Rejections under 35 U.S.C. §103

Claims **1**-5, 7-9, 11 and 14-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawaguchi et al., U.S. Patent No. 5,592,199 (hereinafter "Kawaguchi"), in view of Nakamura et al., U.S. Patent No. 7,136,058 (hereinafter "Nakamura").

Claims 6 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawaguchi in view of Nakamura, and further in view of Kubota et al., U.S. Patent No. 6,791,526 (hereinafter "Kubota").

Applicant respectfully traverses the rejections for the reasons set forth below.

Amended independent **Claims 1 and 7** similarly recite, *inter alia*:

"*an output instruction signal line disposed on the second substrate and opposing the common electrode*;

a timing controller providing a first control signal to the gate driver so as to control an output of the gate driving signal, and providing an output instruction signal to the data driver via the output instruction signal line *to delay the output instruction signal depending on a capacitive load and a resistive load formed by the output instruction signal line and the common electrode*,

wherein the data driver outputs a delayed image data signal to the LCD panel as the output instruction signal is delayed *such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal*."

In a non-limiting embodiment of the claimed invention described at page 13, lines 4-23:

> The gate lines GL and output instruction signal line 510 are formed on the TFT substrate 414, so that *the gate lines GL and output instruction signal line 510 have the capacitive and resistive loads substantially equal to each other.*
>
> Therefore, *the gate driving signal G2 and data signal D2 applied to the second area "B" have a delayed-time of the first time DL1 substantially same as that of the gate driving signal G1 and data signal D1. Also, the gate driving signal G3 and data signal D3 applied to the third area "C" have a delayed-time of the second time DL2 substantially same as that of the gate driving signal G1 and data signal D1.*
>
> Thus, the gate driving signal applied to the gate lines is delayed in a predetermined time according to positions of pixel areas and the data signal applied to the data lines is delayed in the predetermined time, so *that the gate driving signal and data signal may be applied to the pixel areas at the same time.*
>
> As aforementioned above, the LCD apparatus according to the exemplary embodiment of the present invention separately includes the output instruction signal line formed on the TFT substrate on which the gate lines are formed *so as to control the output of the data signal.* The gate lines and output instruction signal line have the capacitive and resistive loads substantially equal to each other because the gate lines and output instruction signal line are formed on a same substrate. Thus, *the output instruction signal has the delayed-time substantially equal to the delayed-time of the gate driving signal applied to the gate line.*

Regarding **Kawaguchi** in the instant Office action at Pages 4, 5 and 7-9, common lines 231, flexible wiring boards 230 along y-axis with six drive IC's 229, and connector 8/control board 232 (Figure 1, Col. 19, lines 15-18/Figure 30, Col. 28, lines 6-14) in Figures 30-32 of Kawaguchi are respectively considered as teaching the "output instruction signal line," the "data TCP," and the "timing controller" of independent Claims 1 and 7.

It is conceded on Pages 4 and 9 of the instant Office action that Kawaguchi does not teach that the timing of the output of image data is according to a delay of the gate driving signal, and it is stated that the resistive load attributed to the metallic signal line which provides the "output instruction signal" in Kawaguchi will *inherently* cause delay and each data driver in Figure 30 of Kawaguchi will be *at least slightly delayed* in outputting the data signal. It is further conceded on Page 5 of the instant Office action, that Kawaguchi does not disclose a common electrode disposed on the first substrate or that the output instruction signal line opposes the common electrode.

Applicant respectfully submits that even if the output instruction signal in Kawaguchi is somehow delayed by the resistive load, the delay is not intentionally disclosed, taught or suggested by Kawaguchi. In contrast, the claimed invention "provides an output instruction signal to the data driver via the output instruction signal line *to delay the output instruction signal depending on a capacitive load and a resistive load formed by the output instruction*

signal line and the common electrode." More particularly, since Kawaguchi does not disclose, teach or suggest an intentional delay, and such a delay of signal line is asserted as being broadly and generally "inherent" due to the material of the signal line, Kawaguchi necessarily *does not teach or suggest* providing an output instruction signal to the data driver via the output instruction signal line **to delay the output instruction signal depending on a capacitive load and a resistive load formed by the output instruction signal line and the common electrode,** and the data driver outputs a delayed image data signal to the LCD panel as the output instruction signal is delayed **such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal** of amended independent Claims 1 and 7.

Since Kawaguchi arguably teaches broadly and generally that an *undefined delay* of a signal line is "inherent" due to the material, there exists *no suggestion or motivation* in the reference or to one of ordinary skill in the art to delay an image signal to the LCD panel "such that **a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal** as claimed.

Regarding **Nakamura** in the instant Office action with respect to independent Claims 1 and 7 at Pages 5, 6, 9 and 10, Nakamura is relied upon as allegedly teaching a common electrode disposed on the first substrate and opposing signal line. At Pages 5 and 10 of the instant Office action, Col. 4, lines 10-19, power supply wiring pattern P1 and capacitor elements C4,C5 wiring in Figures 14 and 15 of Nakamura are relied upon as teaching "signal lines" disposed on the second substrate and opposing the common electrode.

Nakamura teaches signal lines through which an amplified and D/A converted analog *video signal* passes. (See, for example, Col. 4, lines 10-11 and 21-24.) Nakamura teaches *power supply wiring* pattern P1 of AMP 17 which amplifies an output from the DAC 16, overlaps common electrode 23. (See, Col. 15, lines 43-48.) Nakamura further teaches capacitor elements C4 and C5 are connected between stages of inverters IV1 to IV 3 *in the AMP 17*. (See, Col. 15, lines 51-55 and Figure 15.) That is, the lines through which an amplified and D/A converted analog *video signal* passes, the *power supply* wiring P1 and the wiring of capacitor elements C4 and C5 within AMP 17 in Nakamura, does not provide "an output instruction signal" as claimed, which is not a data signal.

As discussed above, the claimed invention "provides an output instruction signal to the data driver via the output instruction signal line *to delay the output instruction signal depending on a capacitive load and a resistive load formed by the output instruction signal line and the common electrode*." In contrast, the lines of Nakamura do not affect the timing of image and data signals. Applicants respectfully submit that Nakamura is silent as to the power supply wiring pattern P1 relative to the common electrode as affecting timing of any signals, let alone data signals.

Therefore, Nakamura *does not teach or suggest* providing an output instruction signal to the data driver via the output instruction signal line **to delay the output instruction signal depending on a capacitive load and a resistive load formed by the output instruction signal line and the common electrode**, and the data driver outputs a delayed image data signal to the LCD panel as the output instruction signal is delayed **such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal** of amended independent Claims 1 and 7, and does not remedy the deficiencies of Kawaguchi.

It is asserted on Page 6 of the instant Office action that the motivation for arranging the signal lines of Kawaguchi so as to overlap the common electrode as taught by Nakamura would be to reduce the frame size of the LCD, resulting in a more portable display, as evidenced by Col. 15, lines 42-50 of Nakamura. Applicants respectfully disagree.

As discussed in the specification of the claimed invention, conventional LCD apparatus produce a waveform of the data signal that is not equal to the waveform of the gate driving signal, and as a result, the gate driving signal may not be applied to the gate lines while the data signal is applied to the corresponding data lines, thereby generating an abnormal image displayed on the display screen of the LCD apparatus. In contrast, the claimed structure of "an output instruction signal line disposed on the second substrate and opposing the common electrode" is specifically intended to control the timing of the image data signal to be more closely associated, e.g., substantially the same, as the timing of the gate signal. Such a purpose of "controlling the timing of the image data signal" is totally unrelated to a purpose of "forming a more portable display."

Therefore, since Kawaguchi teaches an *undefined delay* of a signal line, since Nakamura is *silent* as to the power supply wiring pattern P1 relative to the common electrode as affecting timing of any signals, and since the purpose of "controlling the timing of the image data signal"

is totally unrelated to a purpose of "forming a more portable display" taught by Nakamura, there exists *no suggestion or motivation* in the references or to one of ordinary skill in the art to modify or combine Kawaguchi and Nakamura to provide an output instruction signal to the data driver via the output instruction signal line **to delay the output instruction signal depending on a capacitive load and a resistive load formed by the output instruction signal line and the common electrode**, and the data driver outputs a delayed image data signal to the LCD panel as the output instruction signal is delayed **such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal** of amended independent Claims 1 and 7.

It is conceded on Page 13 of the instant Office action that Kawaguchi does not teach an exact timing of the signal and their application to pixel areas.

Regarding **Kubota** in the instant Office action with respect to Claims 6 and 10, Col. 1, lines 62-67 relative to Figure 14 of Kubota is relied upon as allegedly teaching that a gate driving signal is provided to a corresponding pixel area at a same time as that of the image data provided to the corresponding pixel area.

Figure 14 of Kubota (reproduced below) is a diagram depicting a schematic block diagram of conventional TFT liquid crystal display. Kubota teaches specific gate lines are energized with a timing that corresponds to the control signals from the timing control circuits 5, the TFTs of the pixel cells connected to these gate lines are switched on at the same time, and the drive voltage of each data line is applied to the liquid crystal. (Col. 1, lines 62-67 of Kubota.)

Kubota further teaches in Col. 1, lines 33-55:

> Each gate drive circuit **3** operates such that drive signals for sequentially energizing the gate lines connected to the TFT gates of each row of the pixel matrix are generated in accordance with the control signals from the timing control circuits **5**. The TFTs of the pixel cells lying on the same line are switched on at the same time by the drive signals from the gate drive circuits **3**.
>
> The data drive circuits **4** are configured such that video signals Sc provided in synchronism with a horizontal sync signal are sequentially retained for each of the pixels of the pixel matrix in accordance with the control signals from the timing control circuits **5**, and drive signals for energizing the data lines are generated in accordance with the video signals Sc of the pixels thus retained.
>
> The timing control circuits **5** generate control signals whereby the video signals Sc of individual pixels are sequentially retained by the data drive circuits **4** on the basis of the horizontal or vertical sync signals of the video signals Sc. In addition, each gate drive circuit **3** generates a control signal for energizing the gate line with the timing (horizontal retrace periodicity) at which a video signal Sc corresponding to a single horizontal line is retained by the data drive circuit **4**.

That is, where the specific configuration of Kubota includes video signals Sc presented to the data drive circuits 4 retained by each pixel of horizontal line that corresponds to the control signals from the timing circuits 5, such that the gate lines are energized with a timing that corresponds to the control signals from the timing control circuits 5, Applicant respectfully submits that the configuration of Kubota *does not teach or suggest* providing an output instruction signal to the data driver via the output instruction signal line **to delay the output instruction signal depending on a capacitive load and a resistive load formed by the output instruction signal line and the common electrode** of amended independent Claims 1 and 7, and does not remedy the deficiencies of Kawaguchi and Nakamura.

Furthermore, Applicant respectfully submits that there exists *no teaching, suggestion or motivation* in Kubota or to one of ordinary skill in the art to modify or combine Kawaguchi, Nakamura and Kubota to teach the data driver outputs a delayed image data signal to the LCD panel as the output instruction signal is delayed **such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal** of amended independent Claims 1 and 7.

Thus, since Kawaguchi, Nakamura and Kubota, alone or in combination, *fail to teach or suggest all of the limitations* of similarly amended independent Claims 1 and 7, and since that there exists *no teaching, suggestion or motivation* in the references or to one of ordinary skill in the art to modify or combine Kawaguchi, Nakamura and Kubota to teach the claimed invention, *prima facie* obviousness does not exist regarding at least amended independent Claims 1 and 7 with respect to Kawaguchi, Nakamura and Kubota. Applicant respectfully submits that Claims 1 and 7, and Claims 2-6, 8-11 and 14-17 as respectively depending from Claims 1 and 7, are not further rejected or objected, and are therefore allowable. Entry of the claim amendments, reconsideration, withdrawal of the relevant §103 rejections and allowance of Claims 1-11 and 14-17 are respectfully requested.

Conclusion

All of the objections and rejections are herein overcome. In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. No new matter is added by way of the present Amendments and Remarks, as support is found throughout the

original filed specification, claims and drawings. Prompt issuance of Notice of Allowance is respectfully requested.

The Examiner is invited to contact Applicant's attorney at the below listed phone number regarding this response or otherwise concerning the present application.

Applicant hereby petitions for any necessary extension of time required under 37 C.F.R. 1.136(a) or 1.136(b) which may be required for entry and consideration of the present Reply.

If there are any charges due with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130 maintained by Applicant's attorneys.

Respectfully submitted,

CANTOR COLBURN LLP

By: /Amy Bizon-Copp/

Amy Bizon-Copp
Registration No. 53,993
CANTOR COLBURN LLP
20 Church Street
22nd Floor
Hartford, CT 06103
Telephone (860) 286-2929
Facsimile (860) 286-0115
Customer No. 23413

Date: September 3, 2009